SHIP SYSTEMS INTERFACE USING DIGITAL TECHNIQUES

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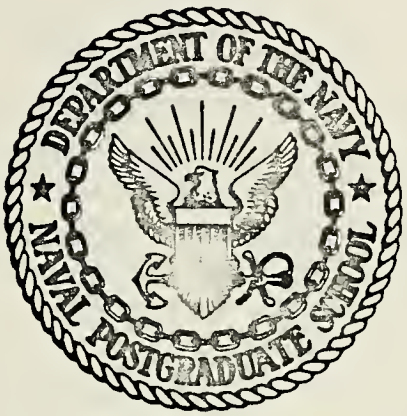

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Using Digital Techniques

by

Donald Ernest Olbert

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The use of a multiple access, time division multiplexed, data bus for interfacing ship systems is developed by first discussing the various sections of such a system and then presenting a system that could be constructed using commercially available components.

The shipboard command and control advantages as well as labor, material and weight savings are discussed in the summary.

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Ship Systems Interface

Using Digital Techniques

by

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Lieutenant, United States Navy
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Submitted in partial fulfillment of the
requirements for the degree of

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ABSTRACT

The use of a multiple access, time division multiplexed, data bus for interfacing ship systems is developed by first discussing the various sections of such a system and then presenting a system that could be constructed using commercially available components.

The shipboard command and control advantages as well as labor, material and weight savings are discussed in the Summary.

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LIST OF ILLUSTRATIONS

ABBREVIATIONS

A/D - Analog to digital

ALU - Arithmetic logic unit

BCD - Binary coded decimal

CMOS - Complementary metal oxide and semiconductor

CPA - Closest point of approach

DTL - Diode-Transistor logic

ECM - Electronic countermeasure

EOT - End of transmission

IC - Integrated circuit

LED - Light emitting diode

LSB - Least significant bit

mA - milliampere

MSI - Medium scale integration

NTDS - Navy tactical data system

ns - nanosecond

ppm - parts per million

RAM - Random access read/write memory

ROM - Read only memory

RPM - Revolutions per minute

SCR - Silicon controlled rectifier

TTL - Transistor-Transistor logic

μs - microsecond

I. INTRODUCTION

In the last five years, the art of digital system and logic design has undergone dramatic changes. Integrated circuits of increasing complexity have not only become available but also cost competitive, creating the opportunity to revise traditional system concepts to minimize total system costs.

The purpose of this paper is to present a digital interface system which could allow shipbuilders to replace thousands of feet of interconnecting cables with a single data bus. This system would also minimize the cost of adding or interchanging sensors and other ship systems since their interface with the rest of the ship would simply be their port on the data bus.

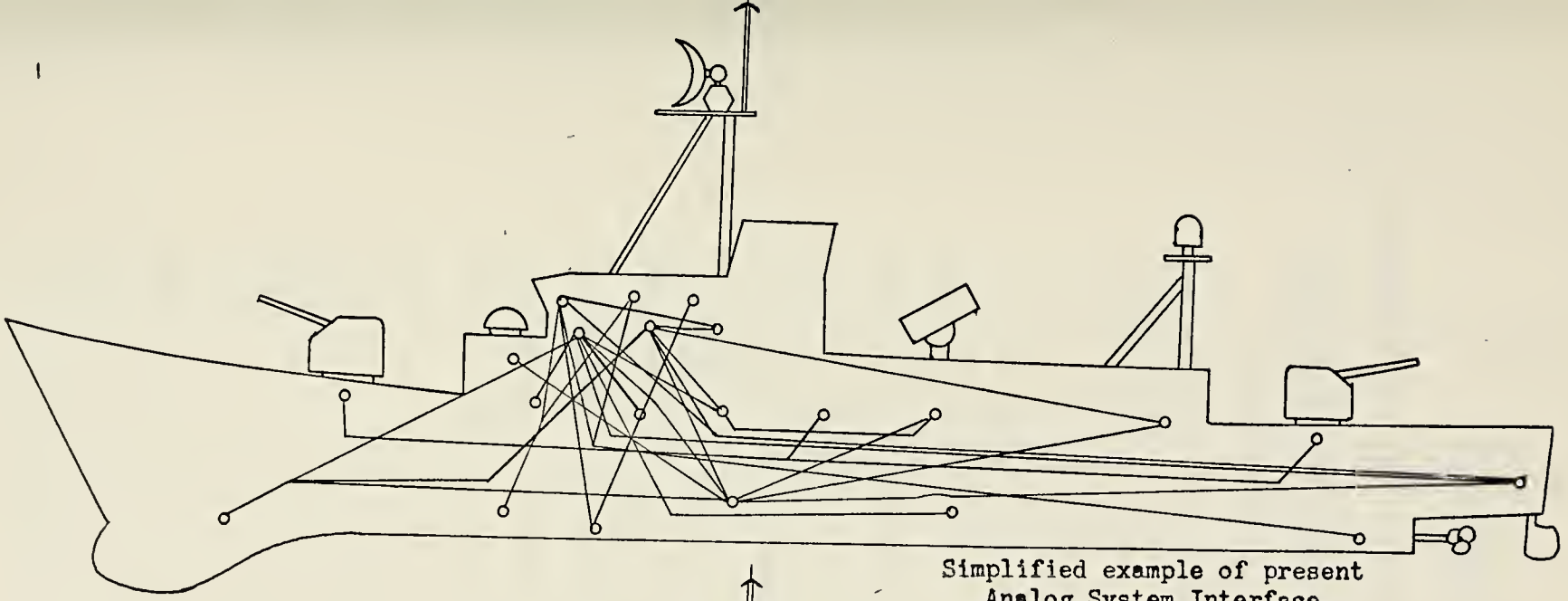
A. ASSUMPTIONS

To provide realistic bounds for development of the system, the following assumptions are made:

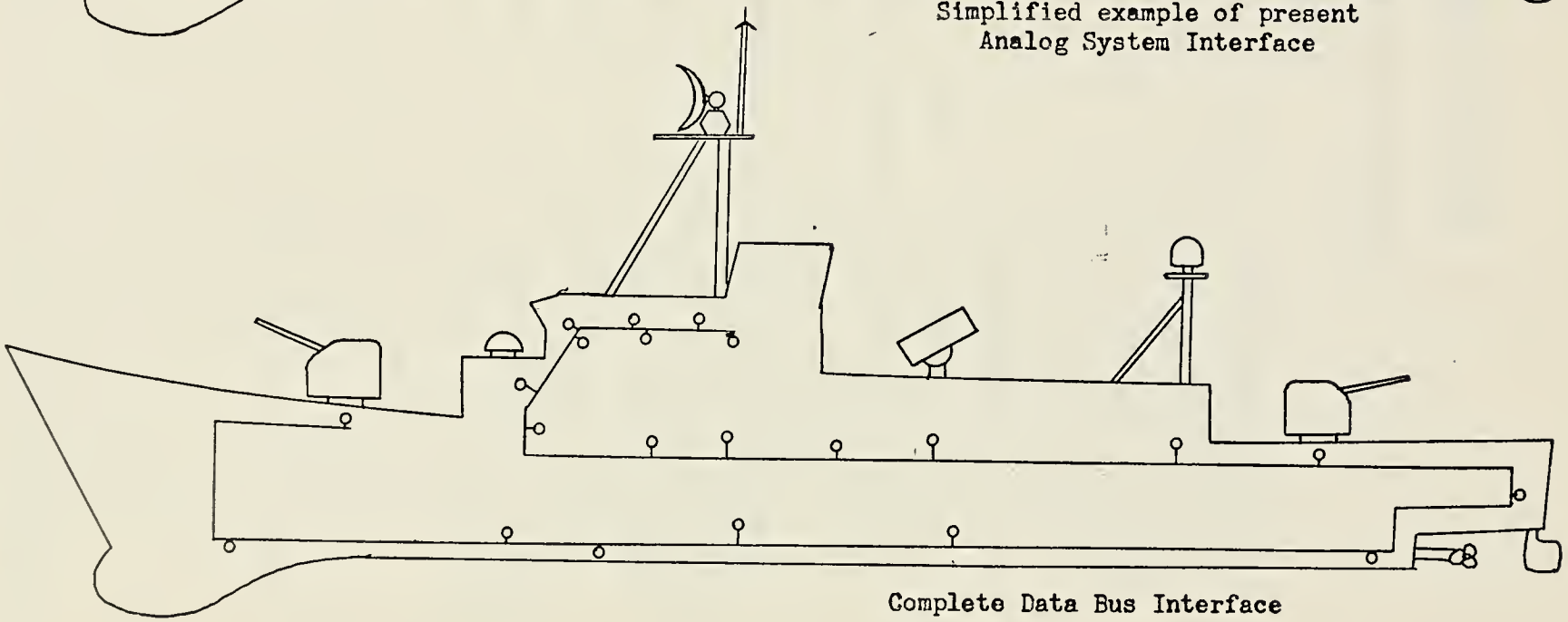
1. Shipboard systems input requirements and output capabilities are as itemized in appendix A.
2. A Destroyer size ship is assumed.
3. Voice Communication Capabilities are not considered.

B. REQUIREMENTS

For the system to be an acceptable replacement for the many analog interfaces that presently exist, no appreciable loss of information content in system outputs can be allowed. Also, the system must be acceptable for use on both NTDS and NON-NTDS type ships.



Simplified example of present
Analog System Interface



Complete Data Bus Interface

II. STATE OF THE ART

A. TRANSMISSION LINE INTERFACE ELEMENTS

1. Design Considerations

The ultimate objective of any system design is to achieve a given performance for the lowest total system cost. This objective may be achieved by the proper selection of system architecture and the selection of those components which are best suited for the system architecture. Today, there is an almost overwhelming variety of alternatives with the several integrated circuit technologies presenting many advantages including increased packing density, reduced interconnections, improved system reliability, reduced power consumption, less heat generation, and decreased design, debugging and service costs. While TTL/MSI circuits are generally accepted in the regular and repetitive portion of digital designs today, the TTL logic cannot normally afford the extra power dissipation required to drive low impedance transmission lines, so line driver circuits are needed to provide the transmission line interfacing. The line driver design must be based on both the form and mode of operation as well as line matching considerations.

2. Forms of Data Communication Circuits

There are two basic forms of data communication circuits, single-ended and balanced differential. The single-ended circuit uses a single line and a common ground return. The advantage of the single-ended system is simplicity with only one signal wire per circuit. The disadvantage is susceptibility to induced noise and ground shift noise. Induced noise is caused by magnetic and capacitive coupling from adjacent signal lines or other noise generators such as brush-type motors or SCR lamp dimmers. Ground shift noise is the result of the voltage potential developed across a ground circuit with a finite resistance and inductance due to flow of current through the ground. The net effect of these noises is that when the signal to noise ratio approaches a value of one, a receiver cannot discriminate between a legitimate signal and a noise voltage which appears to be a signal.

The balanced differential circuit uses a twisted pair of wires as a transmission line, a differential driver, and a differential receiver. The twisted pair transmission line cancel magnetically induced currents in the line because of adjacent twists of the line. Electrostatically coupled noise equally effects both lines of the twisted pair.

Thus it is transformed into a common mode signal at the receiver. A ground shift noise also appears to the receiver as a common mode voltage. Because the signal voltage and noise voltage appear to the receiver as differential and common mode voltages, respectively, they can be seperated by a receiver with high common mode rejection. In this manner, information can be transferred through environments which would otherwise cause errors in single-ended systems.

3. Modes of Operation for Data Communication Circuits

There are two basic modes of operation for data communication circuits, simplex and multiplex. A simplex circuit allows one way, nonreversible data flow whereas a multiplex circuit allows bidirectional or multidirectional non-simultaneous data flow. Some of the multiplex mode operational methods and problems that must be considered are as follows:

a. The protocol or "handshaking" required for a particular port on the bus to send data must be designed. The overall bus operation is either polled or asynchronous. In polled operation, a central bus controller addresses each port in turn to ask if any data is waiting to be sent. If the addressed port has no traffic, it signals "no data" and the controller inquires at the next port.

If the port has some data, then the controller gives a "go ahead" to the port; data is sent, and the controller then inquires at the next port.

In asynchronous operation, any port having data essentially "holds up its hand" and waits for a "go ahead" signal to ripple down the series enabling logic. The priority for a particular port is determined by the port's proximity to the master control port which sends a "go ahead" down the enable logic chain at regular time intervals. This scheme is well suited to bus-organized minicomputers but has some disadvantages for use in a shipboard data interface system where essential control information has no relation to the proximity of the master control port.

b. The effect of powered-down drivers and receivers to normal bus operation must also be considered. Integrated circuit drivers and receivers contain parasitic diodes that are normally reverse-biased when the power supply is on. Unless special design techniques are used, these diodes can become forward biased when the unit is powered-down, thus causing the bus to malfunction.

c. The protocol timing must include sufficient time delays to allow for the different port-to-port signal propagation delays.

d. Both physical ends of the transmission line comprising the bus must be terminated to prevent spurious signal levels due to reflections.

e. Stubs or taps from the main transmission line should be kept to a minimum length. A "daisy chain" wiring method is preferable to a tap off method. If stubs must be used, then to cause the least perturbations on the line, the stub length should be controlled such that the propagation delay of the stub is less than one eighth of the signal rise or fall time at the stub to line connection point.

f. If a three state driver system is used, some means must be provided to detect the differences between a driver sending data and all the drivers in the off condition. In the two state bus system, this problem does not occur because a logic zero indicates either a logic zero or that no port is currently sending.

A logic one on a two state system then indicates a port is transmitting a logic one and the receivers should interpret it as such.

g. Data format considerations include the fact that parallel operation is fast but expensive, since it requires one transmission line and the associated interface for every bit of the word transmitted in parallel. Serial operation is slower, but requires only one transmission line and interface per port. The parallel structure is commonly used for rapid exchange of data over short distances such as within a computer, but the serial structure is used for communications over long distances.

h. A final consideration concerns polled operation of a multiplex system. The amount of time necessary to address and receive acknowledgement from a port must be weighed against the volume of data the ports normally send, and the total number of ports on the bus. If there is a large number of ports on the bus, most of the time might be used by the polling operation with very little time devoted to actual exchange of information.

A large number of ports combined with a high relative volume of traffic expected per port can lead to data backing up at each port waiting to be sent, and an overall reduction in information throughput. In a "real time" system where fast response is essential, serious consideration should be given to splitting up a single large bus into several "satellite busses" each with its own polling controller and protocol with respect to the central bus. Queuing theory can be used to estimate the throughput on a bus structure when many variables including the number of ports, the mean transaction length, and the number of transactions per port per unit of time are known.

4. Component Availability

Many semiconductor manufacturers produce line drivers and receivers designed for a variety of applications. Some typical line drivers designed specifically for bus organized systems are the National Semiconductor DM 7831/DM 8831, DM 7832/DM 8832 TRI-STATE line drivers, and the Fairchild SN 55109/SN 75109, SN 55110/SN 75110 dual line drivers.

Through simple logic control, the DM 7831/DM8831, DM 7832/DM 8832 can be used as either a quad single-ended line driver or a dual differential line driver. The DM 7831 and DM 7832 are specified for operation over the $-55^{\circ}C$ to $+125^{\circ}C$ military temperature range, whereas the DM 8831 and DM 8832 are specified for operation over the $0^{\circ}C$ to $+70^{\circ}C$ temperature range. Key features include: Series 54/74 compatible, 17 ns propagation delay, very low output impedance-high drive capability, 40 mA sink and source currents, gating control to allow either single-ended or differential operation and a high impedance output state which allows many outputs to be connected to a common bus line.

The SN 55109/75109 and SN 55110 are dual line drivers featuring independent channels with common supply voltage and ground terminals. The major difference between the SN 55109/75109 and the SN 55110/75110 drivers is the output current specification. The output current is nominally 6 mA for the SN 55110/75110. The driver circuits have a constant output that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off by appropriate logic levels at the inhibit inputs. The circuit also features an inhibit input that is common to both drivers,

providing more circuit versatility. The common-mode voltage range of the driver outputs is -3V to +10 V, which allows a common mode voltage on the line without affecting the driver performance.

These components are capable of driving a 2000 foot twisted pair, configured as a Balanced-Differential Multiplex bus at a bit rate of 200 K bits per second, with no intersymbol interference.

B. ANALOG TO DIGITAL CONVERTERS

1. Design Considerations

Analog-to-digital converters are encoders that convert analog current or voltage signals to digital codes compatible with the digital system in use. The converters are therefore a key part of the overall data interface system since the digital data being transmitted will be only as accurate as the converters providing the data.

The following parameters are usually considered in the design of A/D converters:

a. Resolution is the relative value of the Least Significant Bit (LSB), or 2^{-n} for n-bit converters. It may be expressed as one part in 2^n, as a percentage, in parts-per-million, or simply by "n" bits.

b. Relative accuracy relates the analog voltage values to the reference used for controlling the slope of the converter transfer function, and is a measure of input/output linearity.

c. Nonlinearity is the maximum deviation from a straight line drawn between the endpoints of the input/output transfer function.

d. Differential Nonlinearity describes the variation in the analog value of transitions between adjacent pairs of digital numbers, over the full range of the digital output.

e. Gain or Scale Factor Stability is defined in terms of the deviation over a given temperature range. The total gain (or scale factor) change is normally specified in ppm/°C.

2. Current Technology

Hybrid technology, presently available in successive approximation type A/D converters, uses thin or thick-film processes to build the necessary integrated arrays of precision resistors. Thick film A/D converters utilize passive elements composed of glass and precious metals fused to a 96% alumina substrate featuring a temperature-coefficient

tracking of 15 ppm/°C and tolerance up to 0.2%. Thin-film devices use nickel-chromium or tantalum nitride resistor layers deposited on silicon. After the circuit has been assembled, the resistors are laser-trimmed with an accuracy to within 0.01%. A temperature-coefficient tracking of 1 ppm/°C is then achieved, resulting in converters with performance specifications that are stable over the entire operating temperature range. The factory trimming also eliminates the need for external adjustments.

Modular fabrication is used in all A/D conversion types, but only a few models of hybrid IC successive approximation converters are currently available.

A recent development in A/D converters uses CMOS technology to produce low power successive approximation modules consuming 30 to 50 mW. In addition to the low power consumption, the hybrid version of these CMOS converters has the adjustment-free capability, which makes these devices highly suitable for many remote applications.

3. Component Availability

The 8-bit A/D Converter shown in figure 2 and the Simultaneous A/D Converter shown in figure 3 are representative of A/D converters that may be designed using available IC components.

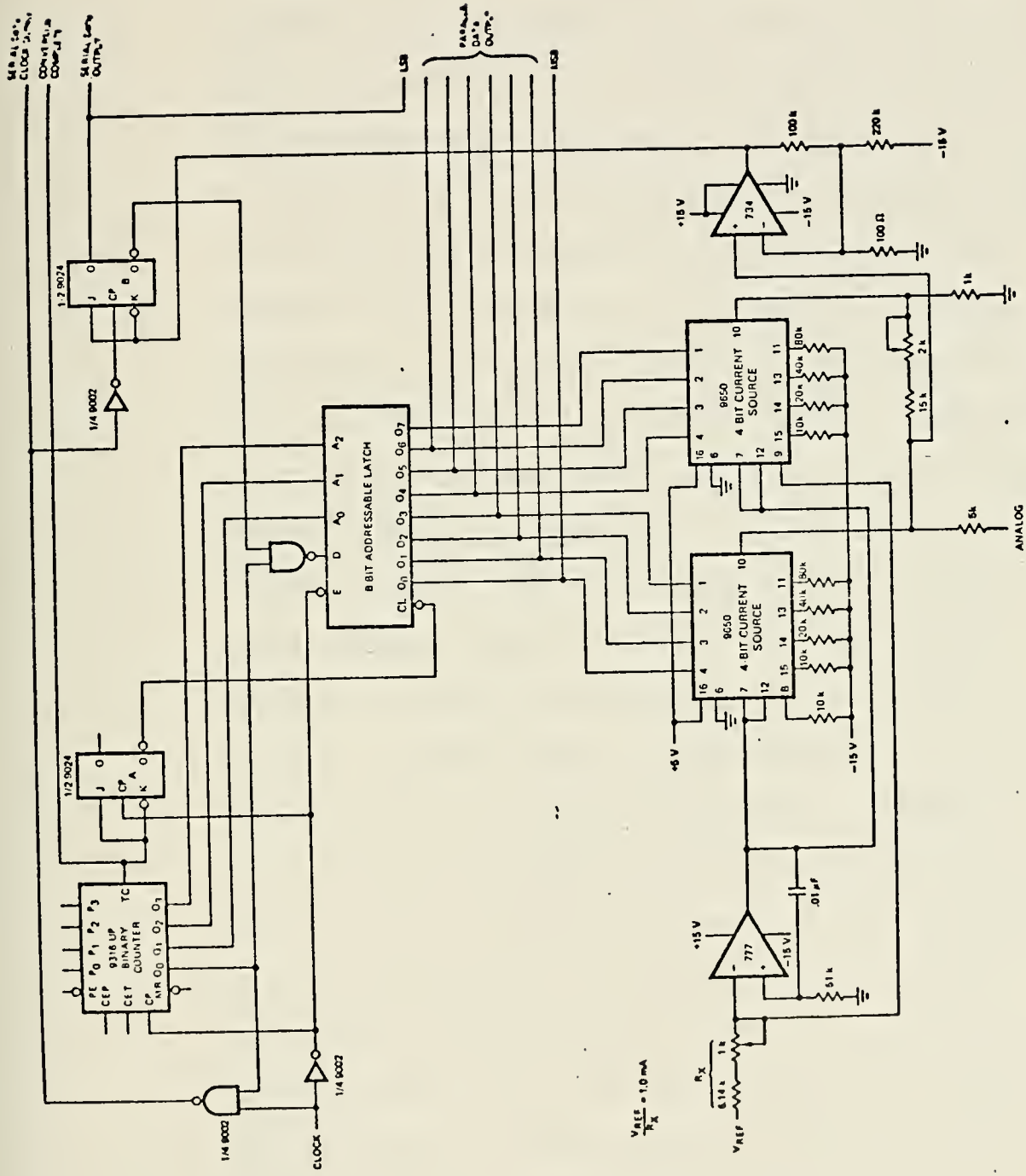


Figure 2. Eight bit A/D Converter

The circuit in figure 2 is an 8-bit successive approximation analog to digital converter. A complete conversion cycle occurs every 16 clock periods with the eight bits generated successively from most significant to least significant bit. During each even clock period the appropriate latch is forced to a one, and during the subsequent odd clock period this latch is conditionally reset. After a one is inserted into a latch the analog equivalent of the 9334 contents is compared with the input voltage. If the 9334 analog equivalent is greater, then the latch is reset; thus, a digital representation is obtained by building up an analog voltage that is compared with the analog input voltage. After 15 clock periods the conversion is complete and during the next clock period, terminal count (TC) can be used to strobe the parallel data from the converter. Serial output data is available and can be clocked from the converter by means of an output clock operating at one half the input clock frequency. Besides the counter and addressable latch, two flip-flops provide delay and isolation. Flip-flop B permits only one logic decision every two clock periods to prevent possible oscillation between the digital and analog circuits and provides the serial output.

The TC output is delayed one clock period by flip-flop A and used to clear the 9334 initializing the conversion cycle. The clock frequency is determined primarily by the fact that the clock must be high longer than the settling time of the linear circuits.

The circuit in figure 3 is one on which fast A/D conversions can be performed by simultaneous multithresholding techniques. In this 3-bit binary A/D converter, the 9318 priority encoder provides all the encoding required. The analog signal voltage to be converted is connected to one input of each analog comparator, while the other input of each analog comparator is connected to one of the seven reference voltages developed in the resistor voltage divider. The input signal is compared to the reference voltage and the comparators generate a high output when the input signal is greater than the reference voltage. The priorty encoder detects the highest order zero, which corresponds to the lowest reference voltage that still exceeds the input voltage. To prevent transient incorrect encoder outputs, while strobing the 9318 outputs, the uA 710 outputs are stored in latches.

The general purpose, low cost A/D converter usually has a resolution of 8 to 12 bits with a

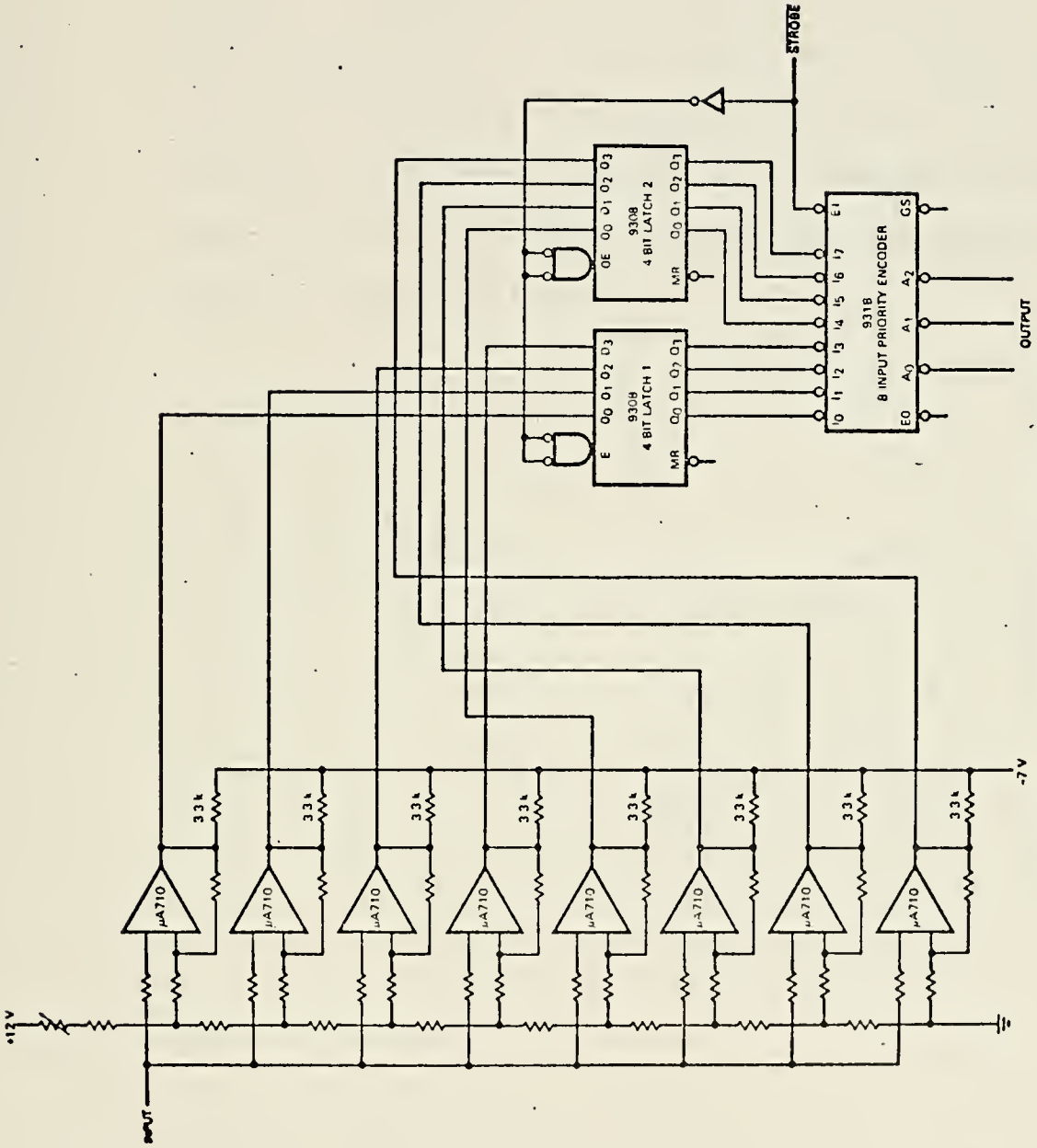


Figure 3. Simultaneous A/D Converter

conversion time of 15 to 100 μs, whereas the high resolution converter may have a resolution of 13 to 16 bits with a conversion time of 8 to 400 μs. High speed A/D converters are available with a resolution of 8 to 12 bits and a conversion time of 1 to 10 μs. The actual selection of each converter must depend on all of the design considerations including resolution, accuracy, conversion time and gain stability.

C. DISPLAY ELEMENTS

1. Design Considerations

After an element of data has reached the systems concerned with that data, it usually is either displayed or utilized as an input variable to the receiving system. As an input variable it might be used in its digital form or converted back to an analog signal, but for display it is usually presented in digital form. There is a wide variety of shapes, sizes, input drive requirements and principals of operation of display units. Most electronic readout devices use neon, fluorescent, incandescent, electroluminescent or gallium arsenide methods to form or illuminate the readout display.

A display decoder/driver takes 4-bit input data and decodes it into the correct format for the particular display being activated. Outputs must be of sufficient current and voltage and correct polarity to drive the display. Such decoder/drivers are now available for many display types in a single integrated circuit.

2. Types of Displays

One of the oldest electronic numeric readouts is the one-of-ten display such as the NIXIE tube.

An inherent disadvantage is that each of the numbers within the tube is not on the same plane. This is very evident when a number of displays are used side by side. Additionally, the red illumination of the displays makes it difficult to change the readout color. Also, they are difficult to multiplex because of relatively high voltage requirements. Seven-segment displays have become popular due to their lower prices and pleasant, modern numeral format. These displays are available in a wide variety of size, color and type.

Incandescent displays can be made in a wide range of sizes and colors and are among the brightest available depending on the lamps used. Until recently their main disadvantage was reliability due to segment failure. New materials, packages and methods however, have improved their reliability.

Many newer incandescent displays have all seven segment filaments contained within a single vacuum envelope and are compatable with standard DTL and TTL voltages. Multiplexing incandescent readouts doesn't offer much advantage in part count as each of the display segments requires a diode to stop sneak electrical paths.

Cold cathode displays, also known as neon, gas discharge, or plasma displays are improved NIXIE type displays with seven segments instead of ten numeral cathodes. Easily read and red-orange in color, they are available in sizes up to 0.75 inches high. They do have a disadvantage in that a high anode potential is required, making them difficult to multiplex.

Flourescent displays are blue-green, available to approximately 0.6 inch character height, and are used primarily in imported calculators. Their relatively low current and voltage requirements make them easy to multiplex.

The light emitting diode is a modern technology, solid state device using either gallium arsenide or gallium arsenide phosphide. Generally, the advantage of these displays lies in their smaller size, more reliable operation under severe mechanical conditions, and voltage current compatability with standard integrated circuit technology. LEDs are available from 0.1 inch to 0.8 inch heights and are typically red in color; however, yellows, greens, and orange are offered at a price. Most of the smaller 0.1 inch LEDs are used in domestic hand calculators.

Liquid crystal displays are unique because they scatter, rather than generate, light. There are two basic types: reflective which requires front illumination, and transmissive which requires rear illumination. Liquid crystal display devices have the lowest power requirements of any display; however, they require an AC drive system which makes them difficult to multiplex. Short operating life, low reliability, and sensitivity to ultra-violet light have impeded the progress of these displays, however, they are rapidly appearing on many battery powered wrist watches.

Other technologies for making seven-segment displays are electroluminescent and light emitting thin films with very high voltage requirements, but IC decoder/drivers for these displays are cumbersome and difficult to make.

3. Display Selection

The type of display to be used depends on a wide variety of factors including type of information, enviornment, speed and power consumption. But, probably most important are the human engineering considerations including readability and comprehensibility. Thus, the shipboard location and use of each display should be considered on an individual basis when designing the display units.

4. Component Availability

The Signetics N7446/N7447 BCD-to- Seven Segment Decoder/Drivers are typical of the readily available devices on the market today. The 7446 and 7447 BCD-to-Seven Segment Decoder/Drivers are TTL monolithic devices consisting of the necessary logic to decode a BCD code to seven segment readout plus selected signs. Incorporated in these devices are blanking circuits allowing leading and trailing zero suppression. Also included is a lamp test control to turn on all segments. The 7446 and 7447 provide bare collector output transistors for directly driving lamps. The output transistor breakdown of the 7446 is 30 volts and the 7447 is 15 volts.

Another example of components on the market today is Signetics DM8880. The DM8880 is a High Voltage Seven-Segment Decoder/Driver designed to decode BCD and drive gas filled seven-segment display tubes.

Decoding is performed by a 16 x 7 read only memory. Thus, for applications desiring other fonts, or applications not using standard BCD inputs, the ROM contents can be altered via metal mask change to produce any seven segment combination for any 16 binary input combinations. The output of the ROM is used to drive high voltage constant current sink generators.

The current sinks will withstand 80 V output. The current sinks are ratioed to the output current as required for even illumination of the segments. Output currents may be varied over a 0.2 to 1.5 mA range through use of the external current programming input. Blanking input provides unconditional blanking of any output display, while the ripple blanking pins allow simple leading or trailing zero blanking.

D. MEMORIES

1. Design Considerations

One of the most basic functions that most digital systems must perform is that of storing information. In a data interface system the storing of information will take place both at the transmitting port prior to transmission, and at the receiving ports after receiving the information.

Bipolar memories fall into two very different categories:

a. Random access read/write memory (RAM) is an array of latches with a common addressing structure for both reading and writing. A "write enable" input defines the mode of operation. In the write mode, the information at the data input is written into the

latch selected by the address. In the read mode, the contents of the selected latch is fed to the data output.

All semiconductor memories have non-destructive readout as opposed to the destructive readout of most magnetic core memories. Bipolar RAM operation is static in that the information is stored in bistable transistor cells and requires no refreshing such as is required in some popular MOS RAMs using capacitor storage. Data in all semiconductor read/write memories can only be stored as long as power is uninterrupted.

b. In a read only memory (ROM), the data content is fixed, normally by a unique metallization of the chip. Addressing is similar to that of a RAM but the operation is static and the readout is non-destructive.

A number of choices must be made in selecting bipolar memory devices for a specific application. The ever increasing need for speed in new designs may impose a propagation requirement on the memory that cannot be met with current TTL technology. This may in turn influence the selection of the logic family used for implementing the ALU or other functions associated with memory.

It should be noted that in the past six years bipolar memory density has increased by a factor of 64, with a corresponding decrease in power per bit without penalizing speed. To assist the engineer in selecting the proper memory device for each application, semiconductor manufacturers provide memory selection guides which correlate the various system parameters to devices and applications.

2. Timing Considerations

A memory system contains many devices for which the delays are different, but the maximum and minimum limits of each must be known. Moreover, when a system is intended for high volume production, the range for the devices to be used in all systems must be known to avoid the need to tune each system individually. A given pair of paths may turn out to have the maximum delay, and for the system to operate reliably, this defines system minimum timing. Yet the designer must also remain aware of the fact that access time may be shorter than the maximum delay and the output of the memory device is then between the maximum and minimum limits of the output delay.

There are eight important memory device delays. These delays are access time, read recovery time, write time, data setup time, data release time, address timing, write recovery time, and chip select delay.

Access time is the length of time from the appearance of a valid address on the address input to the appearance of valid data on the data output, and if specified, the time from the disappearance of the address to the disappearance of the active level.

The read recovery time is the time required for the output of the memory to return to its normal level after the address has been removed. This delay, which is mostly caused by the sense amplifiers inside the device, must be taken into account when two successive read operations from different addresses within a single device cause the data output line to be first low, then high. The high level cannot be attained until after the read recovery time has elapsed.

The write time is the length of time that an active level must be present on the "write enable" to guarantee successful writing in the memory. The system must provide the "write enable" signal for the full length of the write time to guarantee writing in the slowest memory devices. Because the write enable signal begins and ends the writing operation, it is a convenient refcrence for thc other input delays, scrving as a clock or basic timing pulse.

Data sctup time and data releasc time for both high and low output lcvels make up four paramctcrs associated with a mcmory data input. The four sctup

and release times are really only two different quantities, which can have maximum, minimum, and sometimes negative values.

Address timing, like data timing, involves four different quantities, but unlike data timing, both edges of the write enable signal are important relative to the address signal. In most devices, an address is always present on the address inputs, and this must remain unchanged during the write process.

The write recovery time restricts the use of the data output lines following a write operation. It is quite like the read recovery time in that the sense amplifiers respond to the data being written just as they do during a read operation, and when the written data drives the output to its more negative level, the amplifiers require a short time to go positive.

Chip select delay is associated with those memories which have chip select inputs that permit address and data lines to be shared by several chips. One chip can be enabled for a read or write operation.

In designing the timing of a memory system within the framework of the eight device delays, it is best to start by showing all the signals relative to a single time axis in a timing diagram. Only one pulse train can be precisely known at all times, and that pulse train must be taken as the reference. All other signals should be shown relative to the reference.

3. Component Availability

A scratchpad, often called a file, is a small memory integrated into a digital machine and used for temporary storage of current data. Speed is of the essence with cost relatively insignificant. Early files consisted of flip-flop registers, later followed by four to sixteen word RAM or MSI flip-flop arrays. Today there are a number of available scratch pad designs using 16 x 4 TTL RAMs, with files of 256 words or more in development. Main memories vary from 4 K to 16 K bits in minicomputers up to 256 K or more words in large mainframes. Before the availability of bipolar RAMs, system designers were limited to low cost core with one to two microsecond access time, or expensive core with 400 nanosecond to one microsecond access, or MOS with greater than 200 nanosecond access. Some n-channel MOS products promise faster access time at low cost. Present bipolar RAM technology allows implementing large main memories with 70 to 100 nanosecond worst case maximum access times for the subsystem. A read-modify-write cycle of less than 150 nanoseconds is possible using RAM TTL logic.

III. SYSTEM DETAILS

A. COMPONENTS

1. Data Bus

The data bus consists of a pair of RG-131/U balanced twinconductor cables with aluminum armor. The bus cables are operated as balanced differential circuits with one cable containing data transmissions and the other devoted to timing signals. Assuming a bus length of 1500 feet, Alfke and Larsen (Ref.1) report an obtainable NRZ data rate of 250 K bits per second with no intersymbol interference and a minimum pulse width equal to four times the signal rise time. Specifying a 200 K bit system data rate provides a reasonable margin for sustained reliability in the event that one of the transmitting ports is operating at a bit rate up to 12.5% higher than the specified rate. All transmitter and receiver taps should should be kept to a minimum, with none to exceed three inches in length. To provide additional reliability in case of fire or battle damage, two completely separate data busses should be installed on opposite sides of the ship's centerline along with the capability to crossconnect or terminate the bus at each port.

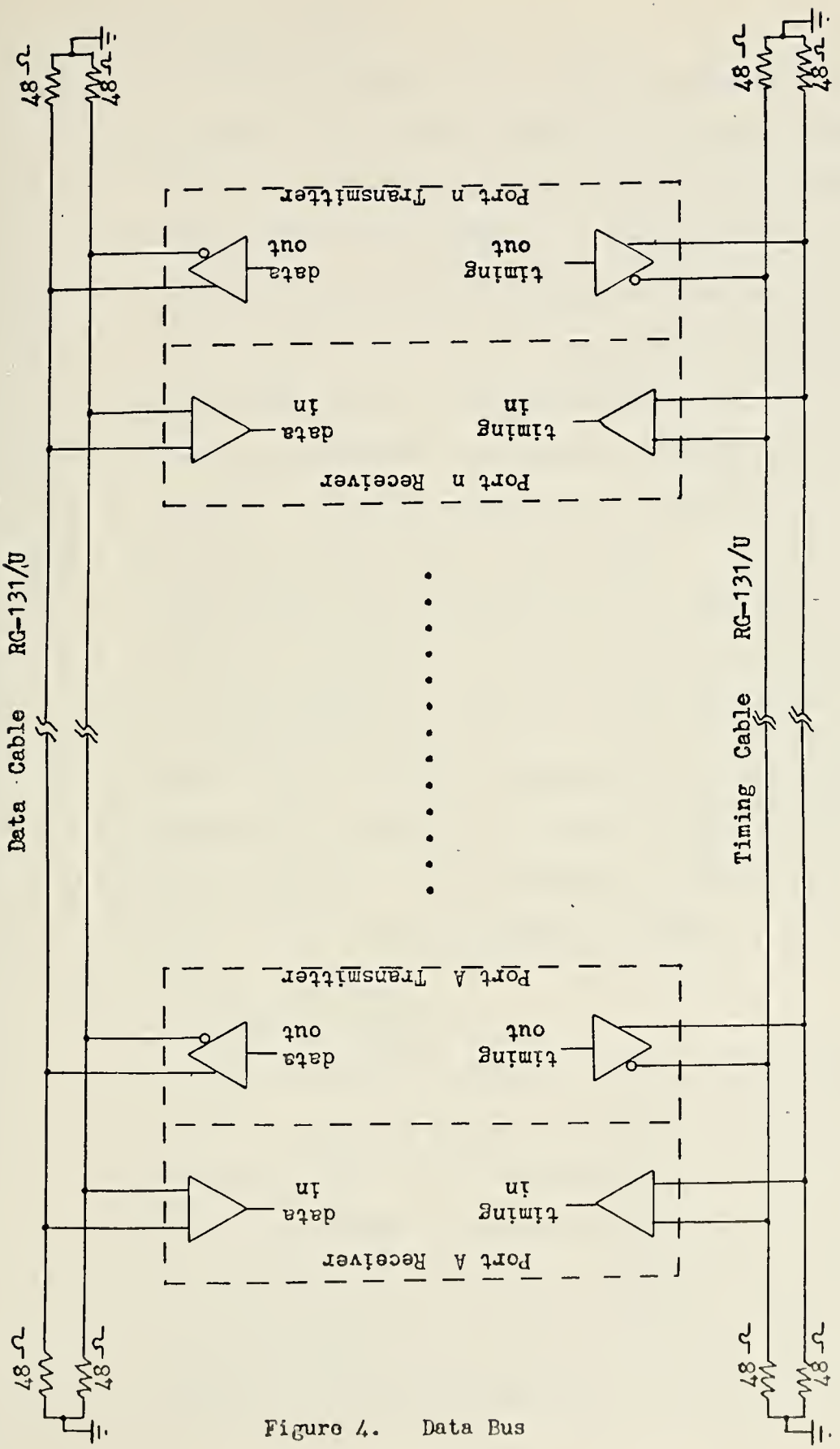


Figure 4. Data Bus

2. Bus Controller

The bus controller utilizes a read only memory to supply the digital "address" of each transmitting station on the bus. Approximately ten microseconds after an EOT signal from one transmitter, the bus controller places the address of the next transmitter on the data bus. If any transmitter does not come on the line within 100 microseconds the bus controller places the address of the same transmitter on the alternate data bus and shows a malfunction indicator specifying the faulty transmitter. If after an additional 100 microseconds the transmitter still does not respond, the bus controller sounds an audible alarm and proceeds to address the remaining transmitters. During shipboard modifications, when systems are added to or removed from the data bus, the addresses of these systems are added to or removed from the bus controller ROM.

3. Transmitting Ports

Each transmitting port has an associated receiving port to monitor the data bus at all times when that port is not transmitting. Upon receipt of its own address, a transmitting port takes control of both the data and timing cables. Approximately ten microseconds after the last bit of address is received, the transmitting port dumps its entire

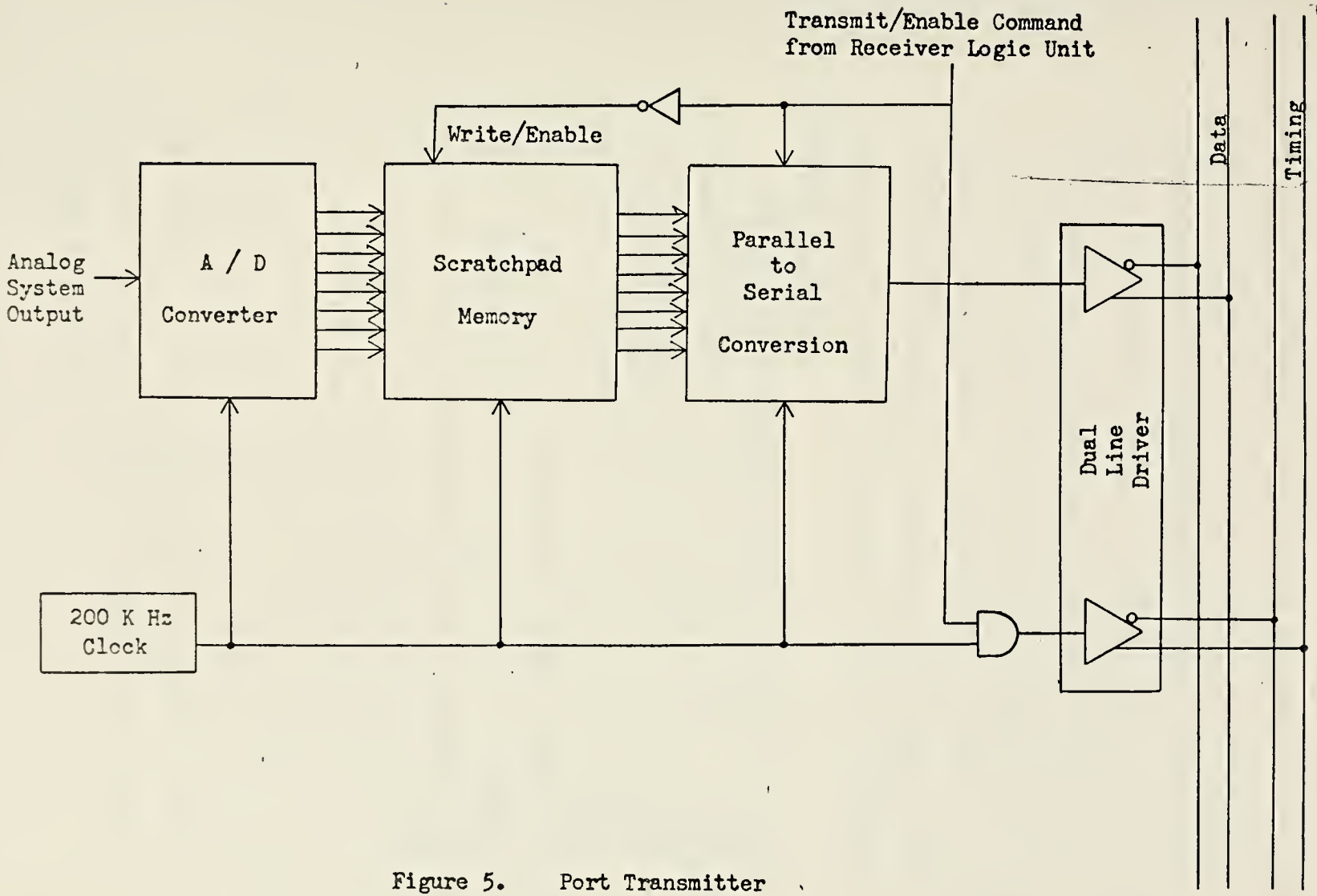


Figure 5. Port Transmitter

output onto the data cable in synchronization with the timing pulses it is placing on the timing cable. Since the data and timing pulses are originating at the same port and propagating down identical cables at the same rate, they will remain in step throughout the entire length of the data bus and the different port-to-port signal propagation delays are inconsequential. Immediately following the data, the transmitting port places an EOT signal on the data bus and then relinquishes control of the bus.

4. Receiving Ports

All ports including the bus controller, data transmitting ports, and data utilization or display ports rely on their receiving port to monitor the data bus. The receiving ports have high input impedance and low input current which induces very little loading on the data bus. The receiving port includes a logic unit which first reviews the address bits to determine if that port is interested in the data to follow, and then routes the data to the appropriate memory location. If the address received is that ports own address, the receiver tells the transmitter to take control and transmit while the receiver waits for the EOT to signal the coming of another address.

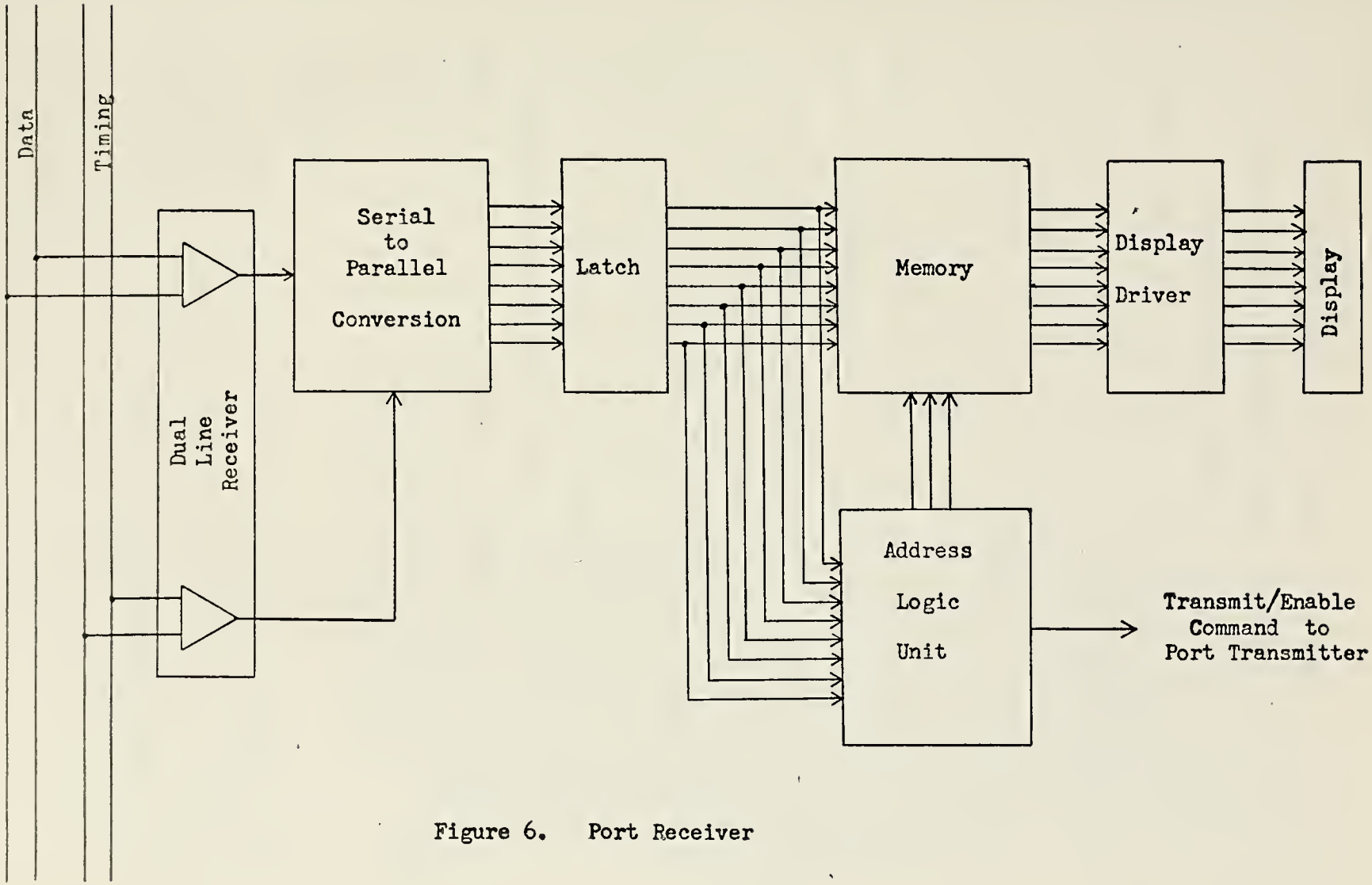


Figure 6. Port Receiver

B. TIMING

In a small digital system a single clock may be utilized to keep all operations in step, and the timing is a relatively simple matter. But, in a shipwide system where the one way transmission delay of a 1500 ft. cable is in the order of 2.55 microseconds and the width of one bit of information is less than five microseconds, it becomes advantageous for each port to contain its own clock. By providing a separate timing cable in the data bus for simultaneous timing and data transmission, no time is lost synchronizing clocks and the coincidence of the timing and data bits are insured regardless of the receiving ports location on the bus. Also, the stability and exact frequency of each clock will not effect system reliability, since the data bits are strobed into all receiving registers by the clock pulses on the timing cable. Once a receiving register is updated and no longer receiving data, that information is utilized or passed to local memory in step with the local clock.

C. OPERATION

The operation of the data system interface is a continuous sequence, controlled by the bus controller. Each system is addressed by the controller and allowed to place its data on the bus before the next system is addressed.

When the controller has received the EOT from the last system on the "list" it starts over and repeats the process indefinitely. While no human operator is required, the controller does provide an alarm in case one of the systems does not respond to its address, in which case corrective action must be taken.

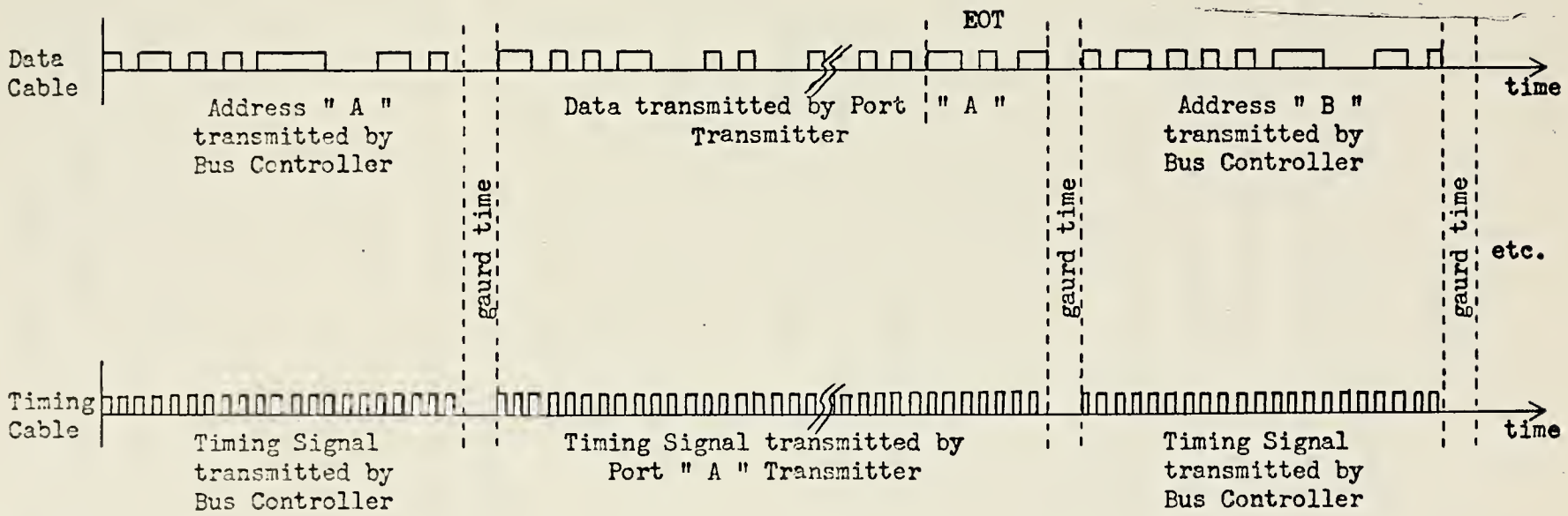


Figure 7. Typical Sequence of Signals Appearing on Data Bus

IV. SUMMARY

A multiple access, time division multiplexed, data bus for interfacing ship systems is not only within the capability of todays technology, but is rapidly approaching the day of becoming a necessity. The data bus operating at a 200 K bit rate would allow each system on a "typical" destroyer sized ship to place its entire output on the data bus at least seven times per second, and make every bit of this information available throughout the ship on a "real-time" basis without phone talkers or other transmitting links. A duplicate port and starboard data bus would require approximately 6,000 feet of RG-131/U cable and would replace somewhere in the order of 30,000 feet of existing multiconductor cables, while providing an interface to which new systems could easily be added without requiring additional cable runs.

It would not be economically feasible to convert existing ships to this type interface system as the cable and installation expense for the existing analog interfaces has already been incurred, but the reduction in weight and cable requirements, as well as reduced installation and conversion costs for ships built initially with the data interface system would more than pay for the system.

The low power requirements of integrated circuit systems allow operation from small battery banks which would

provide uninterrupted service regardless of the status of the ships generators. This, in conjunction with a port and starboard data bus and the capability to cross-connect or terminate the bus at any port, provides a more reliable system overall than the many analog interface systems now in operation.

The final and most important benefit to be derived from the data interface system is a ship which is tied together into a co-ordinated system, more easily controlled by the commanding officer because he has all essential information at his disposal anywhere on the ship without relying on sound powered telephones and other slow questionable sources of information.

SUMMARY OF DATA INTERCHANGE

Data Transmitters \ Data Receivers	Surface Search Radar	Air Search Radar	Sonar	Contact Computer	Fire Control Computer	Conning Officer Control Unit	Rudder Control System	Engine Control System	ECM System	Bridge Status Board	CIC Status Board	CO's Status Board	Wardroom Status Board	Chart Room Status Board	Others
Surface Search Radar				X	X					X	X	X	X		
Air Search Radar				X	X					X	X	X	X		
Sonar				X	X					X	X	X	X		
Contact Computer										X	X	X	X		
Conning Officer Control Unit							X	X			X	X		X	
Rudder Control Unit						X					X				
Engine Control System						X				X	X	X	X		
ECM System				X						X	X				
Fathometer										X	X	X		X	
Barometer and Thermometers					X					X	X	X	X	X	
Anemometer					X					X	X	X	X	X	
Pit Log					X					X	X			X	
Gyro	X	X	X	X	X	X	X		X	X	X	X	X	X	
Ships Clock	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

APPENDIX A.

To develop a realistic data load for the data interface system, shipboard system parameters were established for a "typical" Destroyer sized ship. This was accomplished first by determining the frequency at which each system must place its output on the data bus, and then by calculating the number of data bits required for each output.

To determine the frequency at which each system must place its output on the data bus, the Sampling Theorem was applied to each output along with the conjecture that the system outputs were essentially band limited functions that may be determined by samples that are taken at an average rate of at least two samples per cycle of the maximum frequency content of the output. This minimum sampling rate is known as the Nyquist rate.

To calculate the number of data bits required for each output, the number of significant digits were added to the number of identifying characters required and this total was multiplied by seven to correspond to the seven bit American Standard Code for Information Interchange (ASCII). This code has come into wide acceptance in telegraph and data transmission in the United States and because the equipment to be interfaced comes from a wide variety of manufacturers, the need for standardization of transmission codes is very significant.

The Bus Controller is allotted 21 bits for each call-up command, with a ten micro-second delay between call-up and response. This time delay corresponds to approximately four times the maximum transit time for a pulse to travel the entire length of the 1500 foot data bus, thus insuring that any transits on the bus will be of insignificant amplitude when the data is transmitted. At a system rate of 200 K bits per second the delay corresponds to two bits of time allotted for guard time between each transmission.

The 21 bits of call-up plus two bits of guard time is included in the total data bits required for each system considered in this appendix.

A. SURFACE SEARCH RADAR

1. Outputs

   a. Target designation (three characters)

   b. Target range in yards (six characters)

   c. Target bearing in degrees (three characters)

   d. End of transmission (EOT) one character

2. Data Bits Required

Assuming a maximum antenna rotation rate of 30 RPM and a maximum of 30 targets being tracked at any one time, the surface search radar would require an output frequency of 0.5 outputs per second and a total of 1275 data bits per second or 2550 data bits per transmission.

B. AIR SEARCH RADAR

1. Outputs

a. Target designation (three characters)

b. Target range in yards (six characters)

c. Target bearing in degrees (three characters)

d. Target altitude in feet (six characters)

e. EOT (one character)

2. Data Bits Required

Assuming a maximum antenna rotation rate of 15 RPM and a maximum of 30 targets being tracked at any one time, the air search radar would require an output frequency of 0.25 outputs per second and a total of 952.5 data bits per second or 3810 data bits per transmission.

C. SONAR

1. Outputs

a. Target designation (three characters)

b. Target range in yards (five characters)

c. Target bearing in degrees (three characters)

d. Target depth in feet (four characters)

e. Target doppler (one character)

f. EOT (one character)

2. Data Bits Required

Assuming a maximum of five targets being tracked at any one time and an output frequency of

one update per second, the sonar system will require a maximum of 590 data bits per second or per transmission.

D. SUB-SURFACE / SURFACE / AIR, CONTACT COMPUTER

1. Concept

Especially for the Non-NTDS ship a small digital computer capable of calculating target course, speed and CPA information would be a valuable asset and easily implemented with all of its required inputs already on the data bus.

2. Outputs

a. Target designation (three characters)
b. Target course in degrees (three characters)
c. Target speed in knots (four characters)
d. Target classification (six characters)
e. Target CPA Range in yards (six characters)
f. Target CPA Bearing in degrees (three characters)
g. Target CPA time (four characters)
h. EOT (one character)

3. Data Bits Required

Assuming both radars and the sonar are operating at capacity providing a total of 65 targets, the contact computer will require 13,225 data bits per transmission.

E. CONNING OFFICER CONTROL UNIT

1. Concept

With a fast reliable method of transmitting the conning officers orders to the steering gear room and the engineroom, there is no longer a need for bridge located helm and engine order telegraph. The complete rudder control system can be contained in the steering gear room with the conning officers orders being repeated back by the respective systems. The rudder position and shaft RPM will also be placed on the data bus to be displayed on the bridge and everywhere else desired.

2. Outputs

a. Rudder orders in direction and degrees (three characters).

b. Course to steer to the nearest tenth of a degree (four characters)

c. Engine Orders in direction and amount (ten characters)

d. EOT (one character)

3. Data Bits Required

The conning officer control unit will require 149 bits per transmission.

F. RUDDER CONTROL SYSTEM

1. Concept

In order to give the conning officer the assurance that his orders to the helm were properly received

by the rudder control system, the current orders will be repeated back with each transmission along with the rudder position.

2. Outputs

a. Rudder orders in direction and degrees (three characters)

b. Course to steer to the nearest tenth of a degree (four characters)

c. Rudder position in direction and degrees (three characters)

d. EOT (one character)

3. Data Bits Required

The rudder control system will require 100 bits per transmission.

G. ENGINE CONTROL SYSTEM

1. Concept

In order to give the conning officer the assurance that his engine orders were properly received in the engine room, the current orders will be repeated back with each transmission along with shaft RPM and a composite of the rest of the engineering plant status.

2. Outputs

a. Engine orders in direction and amount (eight characters)

b. Shaft direction and speed (eight characters)

c. Engines on the line (eight characters)

d. Generators on the line (six characters)

e. Fuel percent on board (two characters)

f. Fresh water-percent on board (two characters)

g. Major engineering casualties (ten characters)

h. Sea water temperature in tenth of a degree (three characters)

i. EOT (one character)

3. Data Bits Required

The engine control system will require 359 bits per transmission.

H. ECM SYSTEM

1. Concept

Assuming an integrated ECM system with the capability of matching intercept results with known fingerprints, the important outputs of the ECM system boil down to what and where, thus, all of the individual characteristics of each intercept will not be placed on the data bus.

2. Outputs

a. Intercept designation (three characters)

b. Intercept bearing (three characters)

c. Intercept classification (ten characters)

d. EOT (one character)

3. Data Bits Required

Assuming a maximum of 50 intercepts at any one time, the ECM system will require a maximum of 5630 bits per transmission.

I. FATHOMETER

1. Outputs

a. Water depth in feet (five characters)

b. EOT (one character)

2. Data Bits Required

The fathometer will require 65 bits per transmission.

J. BAROMETER AND THERMOMETERS

1. Concept

By placing all weather information on the data bus, this information is not only continuously available throughout the ship, but also easily recorded and/or transmitted without manual involvement.

2. Outputs

a. Atmospheric pressure in inches (four characters)

b. Dry bulb temperature in tenths of a degree (four characters)

c. Wet bulb temperature in tenths of a degree (four characters)

d. EOT (one character)

3. Data Bits Required

The barometer and thermometers will require a total of 114 bits per transmission.

K. ANEMOMETER

1. Outputs

a. Wind speed in knots (three characters)

b. Wind direction in degrees (three characters)

c. EOT (one character)

2. Data Bits Required

The anemometer will require 72 bits per transmission.

L. PIT LOG

1. Outputs

a. Ships speed through the water in knots (three characters)

b. EOT (one character)

2. Data Bits Required

The pit log will require 51 bits per transmission.

M. GYRO

1. Outputs

a. Ships heading to 0.01 degrees (five characters)

b. EOT (one character)

2. Data Bits Required

The gyro will require 65 bits per transmission.

N. SHIPS CLOCK

1. Concept

To provide a synchronous time base throughout the ship, and electronic clock is a natural source of time data.

2. Outputs

a. Time in hours, minutes and seconds (six characters)

b. EOT (one character)

3. Data Bits Required

The ships clock will require 72 bits per transmission.

0. DATA BUS CONTROLLER

1. Concept

The data bus controller monitors the data bus and after each EOT or any pause greater than 0.1 milliseconds it addresses the next data source. This transmission not only causes the addressed source to transmit, but also opens the receiver gates of those systems interested in that particular data.

2. Data Bits Required

The address or call-up transmissions require 21 data bits for each address. These bits were included in the total data bits required for each of the individual systems.

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